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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,762	11/19/2001	Kenneth Y. Ogami	CYPR-CD01175M	2087

7590 08/10/2006

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EXAMINER	
OSBORNE, LUKE R	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,762	OGAMI ET AL.	
	Examiner	Art Unit	
	Luke Osborne	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/11/2006 has been entered.

Claim Status

2. Claims 1-33 have been presented for reconsideration.

No claims have been added or cancelled. Claims 1-33 are now pending in the instant application.

Applicants' arguments submitted 5/11/2006 have been fully considered, Examiners response is as follows.

Claim Rejections - 35 USC § 101

3. Examiner acknowledges the amendment to Claims 1-14. Consequently the rejection is withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-7, 10-14 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,757,882 to Chen et al. hereinafter "Chen".

Regarding claim 1, Chen discloses a method of matching selectable user module with a plurality of programmable resources associated with an integrated circuit (See the tool as shown in figure 4).

a. Displaying said selectable user module, wherein said user module is representation of a configuration of a programmable circuit (As illustrated, upon invocation, IP package processor 250 (more specifically, description reader 252) identifies and reads basic description 212, block 1302. Description reader 252 then stores the basic information read into corresponding data fields of database 260, block 1304 (Column 9, line 59- Column 10 line 3));

b. In response to a selection of said selectable user module, comparing a description of a hardware resource requirement of said selectable user module with a description of said plurality of programmable resources associated with

said integrated circuit (Next, description reader 252 identifies and reads pins and bus related description 214, block 1308 Figure 13 (Column 10, lines 4-16)); and

c. Using a result of said comparing to identify a first allowed programmable hardware resource on the integrated circuit satisfying the hardware resource requirement of said selectable user module (In response, bus compatibility analyzer 254 determines the bus architectures supported accordingly, including bus signals implemented, and disposition/handling of the unimplemented signals, block 1310 (Column 10, lines 4-16)).

Applicants Argue

Chen fails to disclose comparing a description of a hardware resource requirement of the selectable user module" with a description of the plurality of "programmable resources associated with the integrated circuit".

Examiners Response

Examiner disagrees with Applicants assertion, and find the argument unpersuasive. Rather from Column 13, lines 27-39 states

> For a given base platform design, when it is selected for the SOC design, a customization/configuration menu/form appears, which prompts the designer 202 for inputs for the customizable or configurable attributes of the base platform. Recall that as part of the acquisition process, customizable attribute or parameter information and if applicable, UI element descriptions are read and stored in database 260. In response to the selection of a base platform, the customizable attribute or parameter information, including application UI element descriptions, are retrieved, and customization input forms for prompting a designer 202 to supply the attribute or parameter values are dynamically generated and presented to the designer 202 in order.

This teaches the contented limitations of comparing a description of a hardware resource requirement of the selectable user module" with a description of the plurality of "programmable resources associated with the integrated circuit"

Regarding claim 2 Chen discloses wherein the description of the hardware resource requirement of the user module is represented as XML (For the embodiment, description 210' is expressed using a XML-like Language having XML like language tags defined in accordance with a schema of a namespace associated with Tool Suite 204 (Column 8, lines 23-35)).

Regarding claim 3, Chen discloses wherein the description of the plurality of said selectable programmable resources are represented as XML data (For the embodiment, description 210' is expressed using a XML-like Language having XML like language tags defined in accordance with a schema of a namespace associated with Tool Suite 204 (Column 8, lines 23-35)).

Regarding claim 4, Chen discloses the method according to Claim 1 further comprising highlighting the first allowed programmable hardware resource using a graphical user interface (Upon determining the information, in like manner, bus compatibility analyzer 254 stores the supported bus architecture information, including related synthesized information, into database 260, block 1312 along with figure 6).

Regarding claim 5, Chen discloses identifying a second allowed programmable hardware resource for use with the invention. Figure 7 shows a plurality of memory devices that satisfy the hardware resource of the core being used.

Claim 6 discloses a similar limitation to Claim 4 thus is rejected for the same reasons as claim 4.

Regarding claim 7, Chen discloses the method according to Claim 1 further comprising identifying a disallowed programmable resource on the integrated circuit wherein the disallowed resource represents an unavailable resource on the integrated circuit that otherwise satisfies the hardware resource requirement of the user module (In response, bus compatibility analyzer 254 determines the bus architectures supported accordingly, including bus signals implemented, and disposition/handling of the unimplemented signals, block 1310 (Column 10, lines 4-16) when determining what is allowable the disallowed resources are identified.

Regarding claim 10, Chen discloses the method according to Claim 1 further comprising updating the description of the hardware resource requirement of said selectable user module

> (Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice

elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31)

Regarding claim 11, Chen discloses the method according to Claim 10 wherein said updating is performed in response to changes in a hardware resource requirement of said selectable user module.

(Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31)

Regarding claim 12, Chen discloses the method according to Claim 1 further comprising adding an additional selectable user module to the description of the hardware resource requirement of said selectable user module.

(Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31)

Regarding claim 13, Chen discloses the method according to Claim 1 further comprising updating the description of the plurality of programmable resources associated with said integrated circuit

(Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP

> component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31)

Regarding claim 14, Chen discloses the method according to Claim 13 further comprising adding an additional chip description to the description of the plurality of programmable resource associated with said integrated circuit

> (Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31)

5. Claims 15, 18-24, 26-32 rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pre-Grant Publication No. 2002/0016706 to Cooke et al. hereafter, "Cooke."

Claim 15 recites the apparatus of method claim 18, thus is rejected for the same reasons as claim 18.

Regarding claim 18, Cooke discloses a computer implemented method of determining hardware resources for an electronic design

a) selecting an electronic design [block] represented as a user module of predefined functionality [From the HDL or other high level description, the actual logic

cell implementation is typically determined by logic synthesis, which converts the functional description of the block into a specific circuit implementation of the block. (Paragraph 36)];

b) accessing a data description of hardware resources required for said user module [The computer 110 is preferably coupled to a mass storage device (e.g., magnetic disk or cartridge storage) providing a layout database 195 with which the foregoing system components interface (Paragraph 40)];

c) accessing data descriptions of a plurality of pre-existing programmable hardware resources of an electronic device on which to implement said user module [Floorplan footprints]; and

d) comparing said data description of said user module with said data descriptions of said plurality of pre-existing programmable hardware resources to automatically determine potential placement options of said user module on said electronic device, wherein each potential placement option represents one or more of said pre-existing programmable hardware resources selected to implement said user modeule [At each stage of the design process, as well as at the fabrication stage, various tests may be run to ensure correct operability of the circuit design (Paragraph 36)].

Applicant Argues

Cooke fails to disclose selecting a user module of predefined functionality and implementing the user module on an electronic device that has a plurality of pre-existing programmable hardware resources.

Cooke does not show automatically determining potential placement options of the user module on the electronic device.

Examiners Response

Examiner disagrees with Applicants assertion, and find the argument unpersuasive. Rather from Paragraph [0023] In one step, a foundation block for the integrated circuit is specified, including specifying the locations of multiple androgynous interfaces in the integrated circuit. This foundation block is a selectable user module of predefined functionality.

Cooke shows automatically determining potential placement options and then places them there in the following from paragraph [0043]

> By application of a physical design process 309 shown in FIG. 3, the component blocks of the netlist file 304 are then placed and routed, resulting in a layout file 310. **The component library 306 is utilized in this process stage in order to obtain information concerning the sizes of the components that may be present in the netlist file 304.** Previously, this information includes interface specifications, such as the whether the numbers and locations of the interfaces, whether each interface is a target or initiator, the number of pins and their signal assignments. **As described in the background section above, the placement and routing operation is then performed and may be automated** in a manner to optimize the ICs ultimate performance by minimizing connection lengths and the IC's overall footprint. This placement and routing process however, adheres to the interface specifications obtained from the component library 306.

Regarding claim 19, Cooke discloses the method according to Claim 18 "further comprising:

displaying on a graphical user interface, a first potential placement of said potential placement options; and in response to a user selecting a next placement icon, displaying on said graphical user interface, a second potential placement of said potential placement options [The block placer 130 determines the placement of cells within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Regarding claim 20, Cooke discloses the method according to Claim 19 "wherein potential placement options are displayed using visual attributes and wherein said electronic device is a programmable microcontroller device [Figure 2A Microcontroller item 200]" as claimed.

Regarding claim 21, Cooke discloses the method according to Claim 18 "wherein said user module requires one pre-existing programmable hardware resource to place [Figure 2A item B's]" as claimed.

Regarding claim 22, Cooke discloses the method according to Claim 18 "wherein said user module requires two pre-existing programmable hardware resources to place [Figure 2A item B's]" as claimed.

Regarding claim 23, Cooke discloses the method according to Claim 18 "wherein said plurality of pre-existing programmable hardware resources comprise a plurality of

pre-existing analog programmable hardware resources and a plurality of pre-existing digital programmable hardware resources [The computer 110 may also comprise or be connected to mass storage containing one or more component libraries (not shown) specifying features of electrical components available for use in circuit designs (Paragraph 40)]" as claimed.

Regarding claim 24, Cooke discloses the method according to Claim 18 "wherein said comparing automatically prunes out programmable hardware resources that do not satisfy requirements of said user module

> [The block floorplanner 120 provides for the definition of block functions, block regions, and constraints on these for the purpose of interactive floorplanning operations by the circuit designer, and the control of placement operations of the block placer 130. The block placer 130 determines the placement of cells within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Claims 26-32 recite the system of method claims 18-24, thus are rejected for the same reasons as claims 18-24

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of PSoC Designer: Integrated Development Environment User Guide Revision 1.09, hereinafter "Guide 1.09".

Regarding claim 8, Chen teaches the method according to Claim 7 further comprising distinguishing disallowed programmable resources. Chen does not expressly teach highlighting the disallowed programmable resource using said graphical user interface.

Guide 1.09 teaches that if you attempt to select a User Module that requires more resources than are currently available, PSoC Designer will not allow the selection.

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to use the user feedback of disallowing the selection with the method of Chen.

The motivation for doing so would have been to give the user visual feedback for the operation being performed.

Regarding claim 9, the combination as applied to claim 9 does not expressly teach that the user feedback is highlighting in gray.

Examiner finds this limitation to be design choice, highlight in gray, or graying out is common and is the default for disallowed user feedback in Windows. Furthermore, the method could just have easily picked any other color for indication of such.

7. Claims 16, 17, 25, 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Cooke.

Claims 16, 17 recite the same limitations as claim 25. Thus claims 16 and 17 are rejected for the same reasons as claim 25.

Regarding claim 25 Cooke teaches the method according to Claim 18 wherein the descriptions are represented as data.

Cooke does not expressly teach that the data in the method takes the form of the XML data.

However, these differences from the prior art of record are only found in the nonfunctional descriptive material and do not make a meaningful contribution to the definition of the invention as recited. The limitation of XML does not alter how the method as described in the specification functions. Thus, the identified descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to use XML to store the data in Cooke.

The motivation for doing so would have been to allow the invention as disclosed to be used in various fields of endeavor as the data suggests (XML is a web based technology), thus such data does not alter how the invention functions and the

subjective interpretation of the data does not patentably distinguish the claimed invention. For further evidence of this see Chen above.

Claim 33 recites similar limitations as claim 2, thus is rejected for the same reasons as claim 2.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See form USPTO-892. In particular, U.S. Patent No. 6,353,452 teaches determining automatically and to display distinctly different selections when the selection is not possible. U.S. Patent No. 4,656,603 teaches a GUI with drag and drop interface. U.S. Patent 5,673,198 teaches real time feedback in the design of circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke Osborne whose telephone number is (571) 272-4027. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LRO

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8/6/06